Reg. No.:			9			

Question Paper Code: 30948

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Fifth Semester

Electronics and Communication Engineering

EC 2303 — COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Sixth Semester Biomedical Engineering)

(Regulation 2008)

(Also common to PTEC 2303 – Computer Architecture and Organization for B.E. (Part-Time) Fourth Semester – Electronics and Communication Engineering – Regulation 2009)

Time: Three hours

Maximum: 100 marks

Answer ALL questions.

PART A — $(10 \times 2 = 20 \text{ marks})$

- 1. Write any two types of instruction.
- 2. Let X = 1010100 and Y = 1000011. Perform
 - (a) X-Y and
 - (b) Y-X using 2's complement.
- 3. How overflow is detected in fixed point arithmetic?
- 4. What is the difference between restoring and non-restoring division algorithms?
- 5. Define superscalar processing.
- 6. What is meant by Nano programming?
- 7. What are the advantages of RISC processor?
- 8. What is bus arbitration?
- 9. Differentiate RISC and CISC processors.
- 10. What are vector interrupts?

PART B — $(5 \times 16 = 80 \text{ marks})$

Explain the various addressing modes in detail.

11.

(a)

Or
(b) (i) With suitable example explain fixed point and floating point

(b) (i) With suitable example explain fixed point and floating point number representation in computers. (10)

(ii) Write notes on evolution of computers. (6)

12. (a) Explain 8 bit booth multiplier using flowchart and find the result to multiply $(-22) \times (44)$.

Or

- (b) Explain the algorithm for floating point addition with a flowchart.
- 13. (a) Explain the hardwired and micro programmed control systems. (16)

Or

- (b) Explain instruction pipelining with an example. (16)
- 14. (a) (i) Explain in detail about the replacement policies of memory organization systems. (8)
 - (ii) Give the structure of semiconductor RAM memories. Explain the read and write operations in details. (8)

Or

- (b) Explain in detail about the cache memory organization cache operation and address mapping. (16)
- 15. (a) Stacks and subroutines need passing parameters through registers.

 Justify this statement using suitable calling program and subroutine.

 How I/O operations display few characters or line of characters. What are the various formats for it?

Or

(b) How the different generations evolved paving way to the present generation? What are the features of RISC and CISC processors? How do Dual and Quad processing evolved?